IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method for the planarization of a semiconductor structure having a substrate, in which a plurality of substructures are provided, the substructures having a first substructure, which has planar regions and first trench regions, a layer to be planarized being applied over the semiconductor structure, which layer has corresponding first depressions above the first trench regions of the first substructure, the method comprising the following steps:

(a) ~~preplanarization of~~ preplanarizing the layer to be planarized by an etching step using a preplanarization mask;

(b) ~~subsequent planarization of~~ planarizing the layer to be planarized by a chemical mechanical polishing step;

(c) by means of the preplanarization mask, ~~provision is made of~~ provisioning a first region on the layer to be planarized above the first substructure, which region has a predetermined grid of masked and nonmasked sections;

(d) arranging the masked and nonmasked sections ~~being arranged~~ in such a way that they respectively cover both first trench regions and planar regions;

(e) creating a supporting structure for the chemical mechanical polishing step, which corresponds to the masked sections of the grid, ~~being created~~ by the etching step using the preplanarization mask;

(f) wherein the substructures ~~having~~ have a second substructure, which comprises second trench regions, the layer to be planarized having corresponding second depressions above the second trench regions of the second substructure, and in that, by means of the preplanarization mask, provision is made of a second region on the layer to be planarized above the second substructure, which region is masked throughout; wherein

(i) the first trench regions are capacitor trenches;

(ii) the second trench regions are STI trenches;

(iii) a patterned hard mask is provided on the surface of the substrate, said hard mask being opened at the first trench regions and at the second trench regions;

(iv) the grid of masked and nonmasked sections is a regular grid;

(v) the arrangement of the nonmasked sections have a symmetry, the characteristic lengths of the nonmasked sections being a multiple of the characteristic structure lengths of the underlying first trench regions; and

(vi) the subsequent planarization of the layer to be planarized is effected by a chemical mechanical polishing step as far as the surface of the hard mask.

2. (Original) The method as claimed in claim 1, wherein the second region extends beyond the second trench regions into adjoining substructures.

3. (Original) The method as claimed in claim 1, wherein the substructures have third substructures, which comprise planar regions, and in that, by means of the preplanarization mask, provision is made of third regions on the layer to be planarized above the third substructures, which regions are nonmasked throughout.

4. (Currently Amended) The method as claimed in claim 1, ~~wherein~~ comprising fabricating the preplanarization mask ~~is fabricated~~ lithographically by means of a corresponding photomask on the semiconductor structure.

5. (Currently Amended) The method as claimed in claim 1, wherein the grid has a preferably regular hole structure.

6. (Original) The method as claimed in claim 1, wherein the grid has a preferably regular strip structure.

7. (Original) The method as claimed in claim 1, wherein the grid has at least 50% nonmasked regions.